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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,907	12/06/2001	Charles Neil Stevenson	GP-301468	7209

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EXAMINER	
WORKU, NEGUSSIE	
ART UNIT	**PAPER NUMBER**
2626	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,907	STEVENSON ET AL.	
	Examiner	Art Unit	
	Negussie Worku	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-29* is/are allowed.

6)☒ Claim(s) *30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/06/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 30-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Troxell et al. (USP 6,180,937).

With respect to claim 30, Troxell et al. discloses a method of providing a nondestructive readout of analog data that is representative of the amount of incident light impinging upon a pixel element, (fig 2) comprising the steps of: measuring incident light using a photocapacitor (photocapacitor embodiment 18 of fig 1) that stores charge indicative of the amount of light incident on the photocapacitor (18 of fig 1, see col.3, lines 5-10); transferring the stored charge to a second capacitor (capacitor 18' of fig 5) that is not sensitive to the incident light; and providing the charge stored on the second capacitor (capacitor 18' of fig 5) to an insulated gate of a transistor that is connected to supply an output signal indicative of the voltage on its insulated gate, see (col.4, lines 15-20).

With respect to claim 31, Troxel et al. discloses the method, (fig 1) further comprising the step of gating the output signal using an output transistor, see (col.4, lines18-25).

With respect to claim 32, Troxel et al. discloses the method (fig 1), further comprising the step of dumping the charge stored on the second capacitor (18 of fig 1), to thereby reset the pixel element, see (col.4, lines 20-25).

With respect to claim 33, Troxel et al. discloses the method (fig 1), wherein said steps are carried out using silicon-based electrodes and a silicon-based substrate, (20 of fig 2) and wherein said transferring step further comprises the step of transferring the stored charge between a first depletion region located in said substrate at said photocapacitor, (18 of fig 1) and a second depletion region located in said substrate at said second capacitor (18' of fig 1, see col.4, lines 20-25).

With respect to claim 34, Troxell et al. discloses, wherein said transfer step further comprises using a transfer electrode to create a third depletion region in said substrate (20 of fig 1) that joins said first and second depletion regions, see (col.4, 15-20).

Allowable Subject Matter

With respect to claim 1-15, the prior art searched and of record neither anticipates nor suggests a pixel element for sensing light impinging on the pixel element and providing a non-destructive readout representative of the amount of impinging light, comprising: a substrate capable of forming localized depletion regions in the presence of an applied voltage at the regions; an insulating layer formed on said substrate; a collection capacitor electrode in contact with said insulating layer and being electrically isolated from said substrate by said insulating layer, wherein said insulating layer and collection capacitor electrode are transparent to light; a transfer electrode located adjacent said collection capacitor electrode and being electrically isolated from said substrate by said insulating layer; a readout capacitor electrode located adjacent said transfer electrode and in contact with said insulating layer, said readout capacitor electrode being spaced from said collection capacitor electrode and being electrically isolated from said substrate by said insulating layer; and a readout transistor having an insulated gate connected to said readout capacitor electrode, with said transistor providing an output signal that is indicative of the quantity of charge stored in said substrate under said readout capacitor electrode, whereby said readout transistor provides a non-destructive readout of the stored charge.

With respect to claim 16-18, the prior art searched and of record neither anticipates nor suggests a pixel element for sensing light impinging on the pixel element and providing a non-destructive readout representative of the amount of impinging light, comprising: a silicon-based substrate capable of forming localized depletion regions in the presence of an applied voltage at the regions; a transparent insulating layer formed on said substrate; a first polycrystalline silicon electrode formed as a collection electrode that is transparent to light and that is located within said insulating layer such that it is electrically isolated from said substrate by said insulating layer, said collection electrode being spaced from said substrate such that a first depletion region can be formed in said substrate in response to a bias voltage being applied to said collection electrode, wherein light impinging upon said pixel element at said collection electrode is transmitted through said insulating layer and collection electrode and into said substrate where the impinging light forms electron-hole pairs with the electrons being collected in the substrate near the collection electrode; a second polycrystalline silicon electrode formed as a transfer electrode located laterally adjacent said collection electrode, said transfer electrode being spaced from said substrate by said insulating layer such that a second depletion region can be formed in said substrate in response to a bias voltage being applied to said transfer electrode; a third polycrystalline silicon electrode formed as a readout electrode that is located within said insulating layer such that it is electrically isolated by said insulating layer from said substrate and said collection and transfer electrodes,

said readout electrode being spaced from said substrate such that it provides a readout of charge stored in said substrate under said readout electrode, wherein said second depletion region under said transfer electrode overlaps said first depletion region and permits charged stored in said first depletion region to be transferred to a location in said substrate underneath said readout electrode; a readout transistor having an insulated gate connected to said readout electrode, with said transistor providing an output signal that is indicative of the quantity of charge stored in said substrate under said readout electrode, whereby said readout transistor provides a non-destructive readout of the stored charge; an output transistor having an input connected to said output of said readout transistor, a gate connected to receive a pixel select signal, and an output, with said output transistor being operable to provide said output signal to its output in response to receiving the pixel select signal on its gate; a dump electrode adjacent one of said first, second, and third electrodes; and a supply connecting region in said substrate located adjacent said dump electrode and spaced from said one electrode, wherein, when a bias voltage is applied to said dump electrode with said supply connecting region being connected to a supply voltage, charge stored in said substrate underneath said readout electrode is transferred to said supply connecting region to thereby reset said pixel element.

With respect to claim 19-29, the prior art searched and of record neither anticipates nor suggests a substrate capable of forming localized depletion regions in the presence of an applied voltage at the regions; an insulating layer

formed on said substrate; a collection capacitor electrode in contact with said insulating layer and being electrically isolated from said substrate by said insulating layer, said collection capacitor electrode being spaced from said substrate such that a first depletion region can be formed in said substrate in response to a bias voltage being applied to said collection capacitor electrode, whereby said substrate can store charge supplied to or generated in said first depletion region; a transfer electrode located adjacent said collection capacitor electrode and being spaced from said substrate such that a second depletion region can be formed in said substrate in response to a bias voltage being applied to said transfer electrode; a readout capacitor electrode located adjacent said transfer electrode and in contact with said insulating layer, said readout capacitor electrode being spaced from said substrate such that it provides a readout of charge stored in said substrate under said readout capacitor electrode, wherein said second depletion region under said transfer electrode overlaps said first depletion region and permits charged stored in said first depletion region to be transferred to a location in said substrate underneath said readout capacitor electrode; a readout transistor having an insulated gate connected to said readout capacitor electrode, with said transistor providing an output signal that is indicative of the quantity of charge stored in said substrate under said readout capacitor electrode, whereby data can be temporarily stored in said first depletion region as stored charge which can then be transferred using said second depletion region to a location underneath said readout

capacitor electrode and then used by said readout transistor to provide a non-destructive analog readout of the data.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Negussie Worku whose telephone number is 571-272-7472. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached on 571-272-7471. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER

Negussie Worku
Patent Examiner
Art unit 2626
July 18, 2005